



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,483	10/08/2003	Frederick A. Perner	10014200-1	7466

22879 7590 01/27/2005

HEWLETT PACKARD COMPANY  
P O BOX 272400, 3404 E. HARMONY ROAD  
INTELLECTUAL PROPERTY ADMINISTRATION  
FORT COLLINS, CO 80527-2400

EXAMINER

DICKEY, THOMAS L

ART UNIT PAPER NUMBER

2826

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/681,483

Applicant(s)

PERNER ET AL.

Examiner

Thomas L Dickey

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 December 2004.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 and 21-33 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-5, 7-12, 21-23 and 25-28 is/are rejected.  
7) ☒ Claim(s) 6, 24 and 29-33 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

*Minhloan Tran*  
**Minhloan Tran**  
**Primary Examiner**  
**Art Unit 2826**

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 08 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

Art Unit: 2826

## DETAILED ACTION

1. Applicant's amendment filed 12/10/2004 has been entered.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

- A. Claims 1-5,7-12 and 28 are rejected under 35 U.S.C. § 102(b) as being anticipated by SCHWARZL et al.

Schwarzl et al. discloses a memory with a substrate 21, an array of magnetic memory cells 1,2,3 supported on the substrate 21, each magnetic memory cell 1,2,3 having sides and opposite ends and being adapted to store a bit of information; interconnects 4 in communication with the magnetic memory cells 1,2,3; and conductors WL in communication with the magnetic memory cells 1,2,3 and the interconnects 4, the conductors WL filling spaces between adjacent magnetic memory cells 1,2,3 of the

Art Unit: 2826

array as viewed from the sides of the magnetic memory cells (Note that at least two cells 1-2-3 are stacked one above the other with conductor WL between. Viewed from the side – the horizontal direction – one could see the stacking resulting in vertical adjacency, with WL between) wherein at least one of the conductors WL is deposited on at least one of the interconnects 4 and at least one other of the conductors WL is deposited on at least one of the magnetic memory cells 1,2,3, the conductors WL comprise top conductors (insofar as they are on top of the bottom set of magnetic memory cell 1,2,3), the memory further comprising bottom conductors BL1 disposed generally orthogonally to the top conductors, each bottom conductor supporting multiple magnetic memory cells 1,2,3 of the array, wherein the conductors contact opposite ends of the magnetic memory cells and are disposed along the sides of said cells, and magnetic memory cells 1,2,3 each comprise an active layer having a non-fixed magnetization layer 1 and a reference layer 3 having a fixed magnetization, wherein the conductors WL filling spaces between adjacent magnetic memory cells 1,2,3 of the array are top conductors (again, insofar as they are on top of the bottom set of magnetic memory cell 1,2,3), disposed between bottom conductors BL1 of the array and between the adjacent magnetic memory cells 1,2,3, and wherein each magnetic memory cell 1,2,3 comprises a patterned stack; the memory further comprising a dielectric layer 24-25-26 disposed on sides of the patterned stack and on sides of the conductors WL. Note figure 2, column 5 lines 3367, and column 6 lines 28-38 of Schwarzl et al.

Art Unit: 2826

The applicant's claim 2 does not distinguish over the Schwarzl et al. reference regardless of the process used to form the top conductors, because only the final product is relevant, not the recited process of forming the top conductors by a patterning process that also patterns the magnetic memory cells 9.

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

**B.** Claims 21 and 22 are rejected under 35 U.S.C. § 102(b) as being anticipated by GALLAGHER et al.

Gallagher et al. discloses a memory with means for storing 9 information having logic states, the means for storing 9 comprising a plurality of storage units 8 defining intervening gaps between adjacent storage units 8; and means for sensing 1,2,3,4,5,6 the logic states of the means for storing 9 comprising a plurality of top conductors 4,5,6 and a plurality of bottom conductors 1,2,3 extending generally orthogonally to the

Art Unit: 2826

plurality of top conductors 4,5,6; wherein the means for sensing 1,2,3,4,5,6 fills the intervening gaps of the means for storing 9, and surrounds (as seen from the side, note figures 9-11) the plurality of storage units.

Note figures 1A-1C and column 3 lines 45-67, column 4 lines 5-25, column 5 lines 34-55, and column 6 lines 8 and 9 of Gallagher et al.

C. Claims 23 and 25-27 are rejected under 35 U.S.C. § 102(e) as being anticipated by KIM (6,788,570).

Kim et al. discloses a memory structure, comprising magnetic cells 405 and 411 deposited on first conductive layers 401, the magnetic cells 405 and 411 in communication with first vias (not shown in figure 11 – note column 9 lines 21-22) of the memory structure; insulating layers 407 and 413 deposited on sides of the magnetic cells 405 and 411 and patterned edges of the first conductive layers 401; and second conductive layers 409 and 415 deposited over the insulating layers 407 and 413 and the magnetic cells 405 and 411, the second conductive layers 409 and 415 contacting second vias (not shown in figure 11 – note column 9 lines 21-22) of the memory structure, wherein the second conductive layers 409 and 415 fill gaps between adjacent magnetic cells 405 and 411, multiple magnetic cells 405 and 411 are deposited on a common first conductive layer, and the second conductive layers 409 and 415 form multiple second conductors, directly contacting the magnetic cells 405 and 411 and overlying the second vias, formed from the second conductive layers 409 and 415. Note figure 11, column 8 lines 55-67, and column 9 lines 1-26 of Kim et al. Note that insofar

Art Unit: 2826

as Kim et al. appear to have intended the statement at column 9 lines 21-22 to apply to any memory cells in any of their disclosed memory structures, the memory structures of figures 6,7,8,9, and 10 also appear to anticipate claims 23 and 25-27.

***Allowable Subject Matter***

3. Claims 6, 24 and 29-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

4. Applicant's arguments with respect to claims 1-12,23 and 25-28 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claims 21 and 22 it is argued, at page 9 of the remarks, that "Word and bit lines 1-6 of Gallagher do not surround Gallagher's cells 9." However, when viewed from the sides of magnetic memory cells 9, as on page 8 applicant urges the reader to consider the invention, word lines 4-6, formed under magnetic memory cells 9, together with bit lines 1-3, formed over magnetic memory cells 9, do in fact net out surrounding magnetic memory cells 9. It is only in the three dimensional sense that there is no surrounding.

Art Unit: 2826

### ***Conclusion***

**5. THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For



Art Unit: 2826

more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**TLD**  
**01/05**